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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/079,472	02/19/2002	Maitreyee Mahajani	40025-005	6706

33971 7590 09/16/2003

MATRIX SEMICONDUCTOR, INC.
3230 SCOTT BOULEVARD
SANTA CLARA, CA 95034

EXAMINER
LE, THAO X

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/079,472	MAHAJANI ET AL.	
	Examiner	Art Unit	
	Thao X Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-9,12-15 and 20-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-9,12-15 and 20-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The RCE filed on 04/30/03 was proper and recorded accordingly; thus Advisory Office Action dated 06/18/03 is withdrawn.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 7, 35 is rejected under 35 U.S.C. 102(b) as being anticipated by US 6184155 to Yu et al.

Regarding claims 1, 35, Yu discloses a method for making a transistor containing a gate dielectric structure comprising: providing a gate conductor 5, column 3 line 46, proving a channel (area between source and drain 6/8), and providing between the gate conductor and the channel and in contact with the channel, an oxide layer 4b of the gate dielectric structure by an in-situ steam generation process (ISSP), column 3 line 30-32.

Regarding claims 7, Yu disclose the method wherein the oxide layer 4b having a thickness of about 10 to 20 Angstroms, column 3 line 32.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who

has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1, 6-7, 9, 12-15, 20-21, 24, 26, 27, 30-31 are rejected under 35 U.S.C. 102(e) as being anticipated by US Pub 2003/0017670 to Luoh et al.

Regarding to claim 1, Luoh discloses a method for making a transistor, fig. 1-4 containing a gate dielectric structure, comprising: providing a gate conductor 17 [0018], proving a channel (area between source and drain 19 [0019]), and providing between the gate conductor 17 and the channel an oxide layer of the gate dielectric structure 13 by an in-situ steam generation process (ISSG), fig. 3 step 31 [0020].

Regarding to claims 6-7, 27, 12-15, 20, Louh discloses a method wherein the ISSG is performed at a temperature ranging from 600°C to about 900°C, wherein the pressure ranging from 100 millitorr to about 760 torr [0020], wherein the ISSG oxide layer 13 having the thickness of 10 to about 200 angstrom [0023], wherein the transistor is a SONOS transistor, 10= silicon, 13 = oxide, 14=nitride, 16 = oxide, 17 = silicon [0018], wherein the method further including annealing the oxide layer in a nitric oxide atmosphere [0022].

Regarding to claims 9, 24 Louh discloses a method for making a SONOS device, comprising: providing a channel region (area between source and drain 19 [0019]), and

providing a first oxide layer 13 on the channel region by ISSG process providing a nitride layer 14, on the first oxide layer 13, and providing a second oxide layer 16 on the nitride layer [0020].

Regarding to claim 21, Louh discloses a method for making a gate dielectric structure for a SONOS device comprising: providing silicon 10, providing an oxide layer 13 of gate dielectric structure on the silicon 10 by ISSG [0020], the oxide layer having a thickness of about 10 to 200 angstrom [0023] and annealing the oxide layer in a nitric oxide atmosphere [0022].

Regarding to claim 26, as discussed in the above claims, Louh discloses all the limitations of claim 26.

Regarding to claims 30, 31, Louh discloses the method wherein the silicon is a surface of silicon wafer, wherein the silicon comprises polysilicon. Although the prior art does not specially disclose the claimed silicon wafer, this feature is seen to be inherent teaching of that limitation because the semiconductor substrate 10 would be understood in the art as comprising silicon wafer or polysilicon.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 3, 5, 8, 22-23, 25, 28-29, 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Pub 2003/0017670 to Luoh et al.

Regarding to claim 3, Louh does not expressly disclose the transistor is a thin film transistor (TFT).

However, at the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the ISSG dielectric structure teaching of Louh for intended use. Furthermore, in the recitation 'transistor is a thin film transistor' that has not been given patentable weight because it have been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. Kropa v. Robie, 88 USPQ 478 (CCPA 1951).

Regarding to claims 5, 8, 28, Louh discloses a method wherein the ISSG is performed at a temperature ranging from 600°C to about 900°C, wherein the pressure ranging from 100 millitorr to about 760 torr [0020], wherein the ISSG oxide layer 13 having the thickness of 10 to about 200 angstrom [0023], wherein the transistor is a SONOS transistor, 10= silicon, 13 = oxide, 14=nitride, 16 = oxide, 17 = silicon [0018], wherein the method further including annealing the oxide layer in a nitric oxide atmosphere [0022].

Regarding to claims 22-23, 25 Louh discloses a method for making a gate dielectric structure for a SONOS device comprising: providing a gate conductor 17 [0018], proving a channel (area between source and drain 19 [0019]), and providing between the gate conductor 17 and the channel an oxide layer of the gate dielectric structure 13 by an in-situ steam generation process (ISSG), fig. 3 step 31 [0020], ISSG is performed at a temperature ranging from 600°C to about 1050°C, wherein the pressure ranging from 100 millitorr to about 760 torr [0020], ISSG oxide layer 13 having the thickness of 10 to about 200 angstrom [0023], and annealing the oxide layer in a nitric oxide atmosphere [0022].

But Louh does not expressly disclose the transistor is a thin film transistor (TFT).

However, at the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the ISSG dielectric structure teaching of Louh for intended use. Furthermore, in the recitation ' for transistor is a thin film transistor' that has not been given patentable weight because it have been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. Kropa v. Robie, 88 USPQ 478 (CCPA 1951).

Regarding to claims 29, 32-33, Louh discloses a transistor comprises a floating gate 12, fig. 2.

Regarding to claim 34, Louh does not expressly disclose the gate conductor 17 comprises metal.

But Louh discloses the gate conductor 17 is a conductive layer. At the time of the invention was made; it would have been obvious to one of ordinary skill in the art to replace the conductive gate 17 of Louh with metal, because such substitution would have been considered a mere substitution of art-recognized equivalent values.

8. Claims 39-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6184155 to Yu et al.

Regarding claim 39-42, Yu discloses a method for making a transistor containing a gate dielectric structure comprising: providing a gate conductor 5, column 3 line 46, proving a channel (area between source and drain 6/8), and providing between the gate conductor and the channel and in contact with the channel, an oxide layer 4b of the gate dielectric structure by an in-situ steam generation process (ISSP), column 3 line 30-32, performed at a temperature ranging from 600 to about 1050°C, column 3 line 29, the oxide layer having a thickness of about 10 to 200 angstroms, and annealing the oxide layer in the nitric oxide, column 3 line 28-33.

But, Yu does not the structure for a SONOS device and pressure ranging from about 100 millitorr to about 760 torr.

However, in the recitation 'for SONOS device' in claim 40 and 'a thin film transistor containing a dielectric structure' in claims 41 and 42 that has not been given patentable weight because it have been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. Kropa v. Robie, 88 USPQ 478 (CCPA 1951).

With respect to pressure, it would have been obvious to one of ordinary skill in art to use teaching of Yu in the pressure range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). In addition, the pressure as claimed in the ISSG is commonly used in the art as disclosed by Luoh in US Pub 2003/0017670, [0020] or by Reid in US Pub 2002/0187651, [0013].

9. Claims 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6599801 to Chang et al in view of US Pub 2003/0124873 to Xing et. al.

Regarding claims 36-38, Chan discloses a method for making a SONOS device comprising: providing a channel region (between S/D 312/314), fig. 3, providing a silicon wafer 300, providing a first oxide layer in contact with the channel region or silicon wafer, providing a nitride layer in contact with the first oxide layer, and proving a second oxide layer in contact with the nitride layer, ONO, fig. 3.

But Chang does not disclose a method wherein the oxide layer is a made by an ISSG.

However, Xing reference discloses the method wherein the ONO layer, fig., 2 by ISSG, [0024] and [0025]. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the ISSG teaching of Xing to make the oxide layer as claimed, because it would have created a high quality oxide layer as taught by Xing, column [0002].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X Le whose telephone number is 703-306-0208. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Thao X. Le
August 28, 2003